Design of a 45nm TIQ Comparator for High Speed and Low Power 4-Bit Flash ADC

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Abstract— **The continued speed improvement of serial links and appearance of new communication technologies, such as ultra-wideband (UWB), have introduced increasing demands on the speed and power specifications of high-speed low-to-medium resolution analog-to-digital converters (ADCs).This paper presents the design of high speed and ultra low power comparator of a 4-bit ADC. The comparator used is Threshold Inverter Quantization (TIQ) consuming less than 145μW power with the input frequency of 1GHz and is designed using standard CMOS (Complementary Metal Oxide Semiconductor) technology. The power supply voltage is 0.7V minimum which makes this design adaptable to wide variety of System-on-Chip (SoC) applications. The complete design of ADC is clockless which reduces the electromagnetic interference and gives better modularity. The ADC is targeted for 45nm as it was the mainstream CMOS technology, at the beginning of this research. However, the circuit should be portable to smaller feature size CMOS technologies with lower supply voltages.**

Index Terms— **SoC, CMOS, ADC, TIQ.**

I.INTRODUCTION

ADCs are the key building blocks in many applications including the read channels of magnetic and optical data storage systems, high data rate serial links, high-speed instrumentation, wideband radar and optical communications. With rapid growth of modern communications and signal processing systems, handheld wireless computers and consumer electronics are becoming increasingly popular. These days an ADC becomes a part of System-on-Chip (SoC) instead of a standalone circuit for data converters. To limit energy in a reasonable size battery, minimum power dissipation in the mixed-signal integrated circuits is necessary. The ADC acts as an interface between analog and digital signals. The recent advent of WPAN (Wireless Personal Area Network) standards using high signal bandwidths has necessitated the design of high-speed low-power ADCs. In the initial phase of this work, different architectures of an ADC were studied for their power and speed specifications. It was concluded that Flash ADC is the most appropriate architecture for low power, high speed and medium resolution data converters.

The comparators are the most critical components in a flash ADC. For a n bit flash ADC, an analog input voltage is simultaneously compared with the reference voltage generated by 2^n-1 voltage comparators. The high-speed comparators can be realized with differential amplifiers using bipolar transistors [1]. In this design, the comparators are realized with the inverters, which avoid the complexity in the design of conventional comparators. The Threshold Inverter Quantization (TIQ) technique is used with WPMOS (Width of PMOS) ÷ WNMOS (Width of NMOS) < 1 for all transistors to keep the power consumption as low as possible [2]. The advantage of using these TIQ based comparators over a conventional differential comparator is that a resistor ladder network is not required for providing the reference voltages for the comparators, and the comparison speed is faster. The linearity error against the CMOS process, the power supply voltage and temperature variations are significantly improved by the comparator generation and selection method for the TIQ Flash ADC [9]. In addition, process matching issues are eliminated [2]. This makes the proposed ADC ideal for use in low power high speed System-on-Chips.

II.RELATED RESEARCH WORK

This literature provides a concise study of the work done in the field of ADC designs along with their simulation results and technology used. A TIQ technique is used to model an ADC in [11]. A PRA-ADC is proposed in [4] which enables exponential power reduction with linear resolution reduction. Such a 5 bit ADC is modeled in 180nm technology and has power consumption of 69mW.A TIQ technique has been used to model an ADC in [11]. A flash ADC using TIQ comparator design with 0.7V power supply and power consumption of 11.35mW has been discussed in [5]. An interleaved architecture is used in [6], which is an alternative approach to the parallel architecture used in this paper. A Phase Locked Loop is used to generate clock which is then distributed using different channels and a one channel of 4 bit high speed flash ADC using a 0.18μm CMOS technology is reported. The work in [7] presents a 6-bit 1Gs/sec ADC

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design using TIQ comparator in 45nm CMOS technology. The power consumption reported is 3.875mW. A power saving design by switching half the set of comparators at a time is presented and a power consumption of 40.75mW is reported, simulated in 0.35µm Technology in [3].

This paper presents a design carried out in 45nm CMOS technology, which is the minimum technology currently reported. Moreover, the comparator design consumes power in microwatts and is suitable for high speed SOC applications. The power supply voltage is also the lowest which further supports the recent SOC applications. The comparator is designed to achieve DNL less than 1LSB so that ADC is monotonic [10].The design is simulated in MICROWIND 3.1 [12].

III. TIQ COMPARATOR

A. Introduction to TIQ Comparator

The relentless drive in the semiconductor industry for smaller, faster and cheaper integrated circuits has brought the industry to the 45nm technology node [14]. Hence an effort is made to design this ADC in 45nm technology. Threshold inverter quantization (TIQ) is a unique way to generate a reference voltage for the comparator in a high speed CMOS flash ADC [9]. A TIQ comparator essentially exploits the Voltage Transfer Characteristic (VTC) curve of an inverter as described in Fig.1. By varying its transistor sizes, the comparison voltage can be changed. Fig.1 shows the comparison of the TIQ comparator and a differential voltage comparator in a traditional flash ADC. The circuits are different but the VTC curves are similar.

A key difference between the differential comparator and the TIQ comparator is how to apply their reference voltages. The differential comparator utilizes the external reference voltage (Vr) using a resistor ladder circuit. The Vr directly depends on a resistor tap position. However, the TIQ comparator sets its switching voltage (Vm) internally as the built-in reference voltage, based on its transistor sizes.
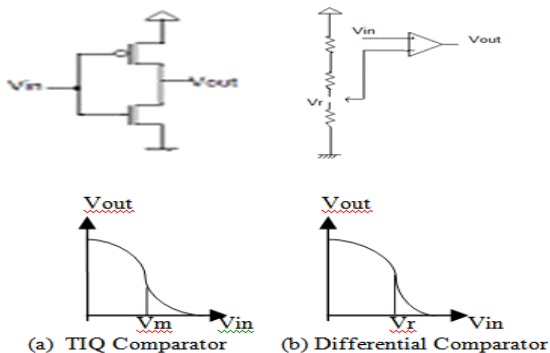
Unlike the conventional flash ADC whose comparators are all identical in size, the TIQ based ADC has individual comparators in all different sizes. To construct an n-bit flash TIQ based ADC, one must find 2^n-1 different inverters, each having different value of switching voltage and one must arrange them in the order of their switching voltage value. The TIQ comparator is a pure inverter circuit; it is inherently faster and simpler than the differential comparator. It has the following features:

i) Clock signals, switches or coupling capacitors are not necessary in the TIQ comparator when comparing the input voltage.

ii) Using standard digital CMOS process makes the TIQ comparator highly suitable for SoC.

B. Design of TIQ Comparator

Implemented flash ADC features the Threshold Inverter Quantization (TIQ) technique for high speed and low power ADC using standard CMOS technology. Fig.2. shows the block diagram of the TIQ comparator. The use of cascading inverters as a voltage comparator is the reason for the technique's name. The voltage comparators compare the input voltage with internal reference voltages, which are determined by the transistor sizes of the inverters. Some of the main problems of the conventional comparator structures used in ADC designs are:

i) large transistor area for higher accuracy,
ii) DC bias requirement,
iii) charge injection errors,
iv) metastability errors,
v) high power consumption,
vi) resistor or capacitor array requirement.

These problems can be overcome by using TIQ. The TIQ technique has many advantages, viz;
i) simpler voltage comparator circuit,
ii) faster voltage comparison speed,
iii) elimination of resistor ladder circuit,
iv) does not require switches, clock signal, or coupling capacitors for the voltage comparison [8].

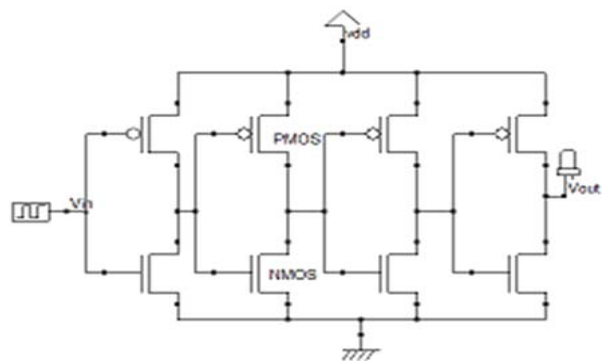Figure.1.The Comparison of TIQ Comparator and Differential Comparator

Figure.2.The TIQ Comparator

Next sub-section explains a very efficient method of designing a TIQ comparator. The design is done such that the comparator consumes minimum power even at high speed.

C. Calculations and Design Considerations of TIQ

The TIQ comparator circuit consists of four cascaded inverters, as shown in Fig.2. The design can also be realized using two cascaded inverters which effectively reduce the chip area [8] but last two inverters shown in Fig. 2. Acts as gain boosters, therefore, four inverters in cascade provide a sharper switching for the comparator and also provide appropriate current to drive the encoder stage. The size of the PMOS and NMOS transistors in a comparator are the same, but they are different for different comparators. They depend upon the switching voltage they are designed for. The mathematical expression used for deciding these switching voltages is given as

$$V_{switching} = \frac{\sqrt{\frac{\mu p Wp}{\mu n Wn}}\left[VDD - |Vtp|\right] + Vtn}{1 + \sqrt{\frac{\mu p Wp}{\mu n Wn}}} \qquad (1)$$

where, Wp = PMOS width, Wn = NMOS width, VDD = supply voltage, Vtn = NMOS threshold voltage, Vtp = PMOS threshold voltage, μn = electron mobility, μp = hole mobility. It is assumed that PMOS length = NMOS length.

It has been stated earlier that a TIQ comparator generates reference voltage internaly, hence the length and width of MOS are varied to get sharper switching at appropriate voltages [13]. One of the techniques of designing the proposed ADC is Systematic Parameter Variation (SPV) technique. In the SPV technique, the length, the width of PMOS and NMOS are varied in order to obtain the desired switching voltage [8]. This technique gives more control on the switching voltage of the individual comparator but generates a complex design. Since the comparator stage depends on threshold voltage of PMOS and NMOS, a robust design was critical to ensure that the practical threshold voltages would not deviate too much from the design and the power consumption is reduced drastically.

Firstly, the transistor channel length was considered. A very small value would result in high speed but the output would be affected by shot channel noise, which would give non linear switching pattern. Therefore, an equal length of 0.080μm for both PMOS and NMOS was decided after testing with various designs. Secondly, increasing Wp (while Wn is constant) shifts the static characteristics of an inverter to a higher voltage which gives the switching voltage of the next comparator.

In contrast to the SPV Technique, Wp was systematicallyvaried and all the other parameters were kept constant. The general approach was to keep WPMOS÷WNMOS < 1 to reduce power consumption and also reduce the parasitic capacitances.

Thus, for all the inverters WNMOS was kept constant and WPMOS was adjusted to achieve the measured switching values approximately equal to the calculated switching values. In this design, low leakage current MOS devices are used in order to keep the power consumption as small as possible.

The sizes of the NMOS and PMOS transistors used in the proposed ADC corresponding to the minimum and maximum switching voltages are shown in Table I. The comparator switching voltage results in a least significant bit (LSB) of 0.02V. Although, repeated efforts were made to make sure that the calculated and the observed switching voltages were same for every comparator, minute difference between the two values was observed. This difference occurs because only WPMOS was varied, so it becomes difficult to achieve the calculated voltage. Moreover, difference between the calculated and the observed switching voltage is not more than 10%, which is under tolerable limits.

TABLE I
SIZES OF THE TRANSISTORS FOR SWITCHING VOLTAGE FOR 4-BIT FLASH ADC

Comparator No	Wp (μm)	Wn (μm)	Vswitching (V)
1	0.08	0.08	0.318
2	0.12	0.08	0.343
3	0.16	0.08	0.375
4	0.24	0.08	0.399
5	0.28	0.08	0.418
6	0.74	0.08	0.434
7	0.76	0.08	0.462
8	1.40	0.08	0.480
9	2.20	0.08	0.497
10	6.00	0.08	0.515
11	14.0	0.08	0.534
12	24	0.08	0.550
13	50	0.08	0.581
14	60	0.08	0.600
15	70	0.08	0.620

IV. SIMULATIONS AND RESULTS

The transient analysis of the TIQ comparator was performed. The comparators have been designed using semi-custom design technique in Microwind 3.1. Mask layout of the comparator section is shown in Fig. 3. A semi-custom design approach was followed to generate the mask layout wherein a careful placing and routing was done so as to;
(i) reduce noise interference,
(ii) reduce overall power consumption of all the comparators,
(iii) reduce global crosstalk delays,
(iv) minimize load capacitance.

The simulation results show distinct switching of each comparator as shown in Fig.4. The input signal has a

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bandwidth of 1GHz. The complete ADC consumes power less than 145μW and covers surface area of 837μm². The ADC so designed reported a speed of 2.2 Gs/sec. The DNL is less than 0.5 LSB and INL is less than 0.7 LSB which is within acceptable limits to guarantee monotonocity of the ADC and avoid metastable states. The entire design is simulated in Microwind 3.1. Thus it can be observed from the simulation results that, the analog input is successfully converted to 15 bit digital output.
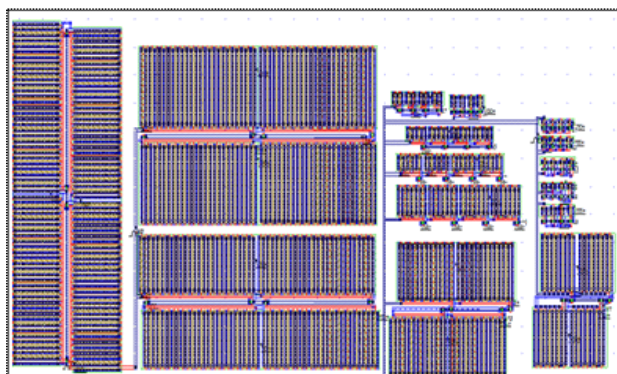

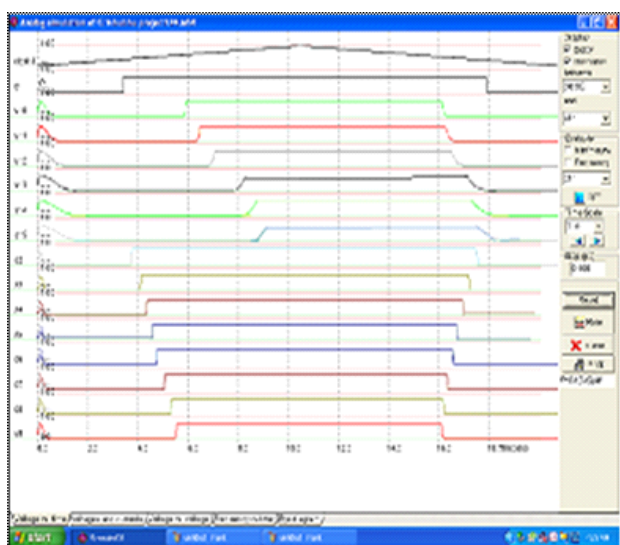Figure.3. Mask Layout of 4-bit TIQ

Figure.4. Different switching voltage of 4-bit ADC

V.CONCLUSION AND FUTURE SCOPE

The design and simulation results of 4-bit Flash ADC using 45nm latest technology have been presented. In addition, it has been shown that, the power consumption is substantially reduced and the speed is considerably increased. The power supply voltage is substantially reduced to 0.7V thereby making the design adaptable for high speed SoC applications. Moreover, it is worth noting that the proposed ADC is a clockless circuitry, which is also a reason for the reduced power consumption. However, we further plan to integrate the comparator of an ADC with a high speed encoder mainly the Fat-Tree Encoder. Thus, an ADC which is functional at nanoscale CMOS technologies has been successfully designed and demonstrated.

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